



**NEHRU COLLEGE OF ENGINEERING AND RESEARCH CENTRE  
(NAAC Accredited)**

(Approved by AICTE, Affiliated to APJ Abdul Kalam Technological University,  
Kerala)



**DEPARTMENT OF ELECTRONICS & COMMUNICATION  
ENGINEERING**



**SYLLABUS BOOK FOR STUDENTS**

**M.TECH VLSI SYLLABUS HANDBOOK**



**VISION OF THE INSTITUTION**

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

**MISSION OF THE INSTITUTION**

**NCERC** is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

**ABOUT DEPARTMENT**

◆ Established in: 2002

◆ Course offered : B.Tech in Electronics and Communication Engineering

M.Tech in VLSI

◆ Approved by AICTE New Delhi and Accredited by NAAC

◆ Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

## **DEPARTMENT VISION**

Providing Universal Communicative Electronics Engineers with corporate and social relevance towards sustainable developments through quality education.

## **DEPARTMENT MISSION**

- 1) Imparting Quality education by providing excellent teaching, learning environment.
- 2) Transforming and adopting students in this knowledgeable era, where the electronic gadgets (things) are getting obsolete in short span.
- 3) To initiate multi-disciplinary activities to students at earliest and apply in their respective fields of interest later.
- 4) Promoting leading edge Research & Development through collaboration with academia & industry.

## **PROGRAMME EDUCATIONAL OBJECTIVES**

PEO1. To prepare students to excel in postgraduate programmes or to succeed in industry / technical profession through global, rigorous education and prepare the students to practice and innovate recent fields in the specified program/ industry environment.

PEO2. To provide students with a solid foundation in mathematical, Scientific and engineering fundamentals required to solve engineering problems and to have strong practical knowledge required to design and test the system.

PEO3. To train students with good scientific and engineering breadth so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.

PEO4. To provide student with an academic environment aware of excellence, effective communication skills, leadership, multidisciplinary approach, written ethical codes and the life-long learning needed for a successful professional career.

## **PROGRAM OUTCOMES (POS)**

### **Engineering Graduates will be able to:**

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

#### **PROGRAM SPECIFIC OUTCOMES (PSO)**

**PSO1:** Ability to Formulate and Simulate Innovative Ideas to provide software solutions for Real-time Problems and to investigate for its future scope.

**PSO2:** Ability to learn and apply various methodologies for facilitating development of high quality System Software Tools and Efficient Web Design Models with a focus on performance optimization.

**PSO3:** Ability to inculcate the Knowledge for developing Codes and integrating hardware/software products in the domains of Big Data Analytics, Web Applications and Mobile Apps to create innovative career path and for the socially relevant issues.

**APJ ABDUL KALAM TECHNOLOGICAL  
UNIVERSITY**

**SCHEME AND SYLLABY FOR  
M. TECH.  
in  
VLSI**

## SEMESTER 1 (CREDITS: 22)

Exam Slot	Course No	Course Name	L-T-P	Internal mark	End semester exam		Credit
					Marks	Duration (hrs)	
A	08 EC 6311	Advanced Engineering Mathematics	3-0-0	40	60	3	3
B	08 EC 6321	CMOS VLSI Design	4-0-0	40	60	3	4
C	08 EC 6331	Advanced Digital System Design	3-0-0	40	60	3	3
D	08 EC 6341	VLSI Fabrication Technology	3-0-0	40	60	3	3
E	08 EC 6351	Elective 1	3-0-0	40	60	3	3
	08 GN 6001	Research Methodology	0-2-0	100	0	0	2
	08 EC 6371	Seminar		100	0	0	2
	08 EC 6381	VLSI Design lab	0-0-2	100	0	0	2
<b>Credits</b>							<b>22</b>

L-Lecture T- Tutorial P- Practical

### ***ELECTIVE 1***

1.08 EC 6351(A): Electronic System Design

2. 08 EC 6351(B) :Digital Integrated Circuits Design

3.08 EC 6351(C): Designing with microcontrollers

## SEMESTER 2 ( CREDITS : 19)

Exam Slot	Course No	Course Name	L-T-P	Internal mark	End semester exam		Credit
					Marks	Duration (hrs)	
A	08 EC 6312	Analog VLSI Design	3-0-0	40	60	3	3
B	08 EC 6322	CAD of VLSI Circuits	3-0-0	40	60	3	3
C	08 EC 6332	Testing and Verification of VLSI Circuits	3-0-0	40	60	3	3
D	08 EC 6342	Elective 2	3-0-0	40	60	3	3
E	08 EC 6352	Elective 3	3-0-0	40	60	3	3
	08 EC 6362	Mini Project	0-0-4	100	0	0	2
	08 EC 6372	Testing and Verification of VLSI Circuits lab	0-0-2	100	0	0	2
<b>Credits</b>							<b>19</b>

**L-Lecture T- Tutorial P- Practical**

### **ELECTIVE 2**

1.08 EC 6342(A) :Low Power VLSI Design

2.08 EC 6342(B): Synthesis and Optimization of Digital Circuits

3.08 EC 6342(C): Design of Digital Signal Processing

### **ELECTIVE 3**

1.08 EC 6352(A):High Speed Digital Design

2.08 EC 6352(B): SoC Design and Verification

3. 08 EC 6352(C):Nano electronics

### SEMESTER 3 (CREDITS: 14)

Exam Slot	Course No	Course Name	L-T-P	Internal mark	End semester exam		Credit
					Marks	Duration (hrs)	
A	08 EC 7313	Elective 4	3-0-0	40	60	3	3
B	08 EC 7323	Elective 5	3-0-0	40	60	3	3
	08 EC 7333	Seminar	0-0-2	100	0	0	2
	08 EC 7343	Project Phase I	0-0-12	50	0	0	6
<b>Credits</b>							<b>14</b>

L-Lecture T- Tutorial P- Practical

#### Elective 4

1.08 EC 7313(A): FPGA Architecture and Application

2.08 EC 7313(B): Mixed Signal System Design

3. 08 EC 7313(C): ASIC Design

#### Elective 5

1. 08 EC 7323(A): System Verilog

2. 08 EC 7323(B): Hardware Software co design

3. 08 EC 7323(C): VLSI Signal Processing

**SEMESTER 4 (CREDITS: 12)**

Exam Slot	Course No	Course Name	L-T-P	Internal mark	End semester exam		Credit
					Marks	Duration (hrs)	
	<b>08 EC 7314</b>	Project Phase II	0-0-21	70	30	0	12
<b>Credits</b>							<b>12</b>

**Total Credits : 67**



## 08 EC 6311 ADVANCED MATHEMATICS

Credits: 3-0-0: 3

Year: 2015

Pre-requisites: Nil

### Course Objectives:

To give the Student:-

- In-depth of understanding of signal transforms and representations
- A detailed treatment on linear algebra equips the student with subtle skills required to understand the wavelet transforms

### Syllabus

Fundamental concepts and overview; Laplace transform, fourier transform, Linear equations and Matrix Algebra, Introduction, 2D orthogonal & unitary transform, Wavelet Transform

### Course Outcome:

On successful completion of this subject, students should be able to

- Apply transform techniques effectively for analysis of signals and systems
- Utilize effective arithmetic using floating points systems and standard
- Apply effective linear algebra such as linear equations and matrix operations for analysis of problem
- Apply multidimensional transforms for signal and image processing

### TEXT BOOKS:

1. "Linear Algebra and its Applications", David C. Lay, 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005
2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier
3. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi

### REFERENCE BOOKS:

1. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists, Murray R. Spiegel, MGH Book Co., New York
2. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK
3. Advanced Engineering Mathematics, JAIN, R K, IYENGAR, S R K, Narosa, NEW YORK

## COURSE PLAN

<b>08 EC 6311 ADVANCED MATHEMATICS (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Laplace Transform - Definition - Transforms of elementary functions First shifting Theorem – Change of scale property - Inverse Laplace Transform - Laplace Transform of derivatives - Laplace Transform of Integrals - Multiplication by $t^n$ - Division by $t$ - Convolution Theorem - Application to differential equation	<b>6</b>	<b>15</b>
<b>MODULE:2</b> Fourier Transform – Transforms of elementary functions – Properties of Fourier Transform – Fourier cosine & sine Transform – Z – Transform - Definition – properties – Initial value Theorem - Final value Theorem – Methods to find Inverse Z – Transform – Application of Z – Transform to difference equation.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE:3</b> Linear equations and Matrix Algebra – Fields – System of linear equations and its solution sets – Elementary row operations and echelon forms – Matrix operations – Invertible matrices – LU Factorization Vector Space – definition & examples – subspaces – bases – dimension – coordinates	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Introduction, 2D orthogonal & unitary transform, properties of unitary transforms 1D and 2D - DFT, DCT, Walsh, Hadamard Transform, Haar Transform, Slant transform, KLT, SVD Transform	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Wavelet Transform: Continuous: introduction, C - T wavelets, properties, inverse CWT, redundancy issue	<b>7</b>	<b>20</b>
<b>MODULE :6</b> Discrete Wavelet Transform: introduction, Vector spaces and MRA, orthogonal wavelet decomposition using Haar Wavelets, bi-orthogonal wavelets.	<b>8</b>	<b>20</b>

## 08 EC 6321CMOS VLSI DESIGN

**Pre-requisites:** Nil

**Credits:** 4-0-0: 4  
**Year:** 2015

### **Course Objectives:**

- To design and develop the CMOS circuits and system with subsystems
- To interpret and analyze the basic characteristics of CMOS

### **Syllabus**

MOS device design equations, DC characteristics, CMOS logic structures, design strategies, verification and testing, Data path operation, multiplication, and memory elements control FSM

### **Course Outcome:**

Upon completion of the course, student will be able to design and develop simple circuits for a processor with CMOS Technology

### **TEXT BOOKS:**

1. Neil. H.E. Weste and K. Eshragian, "Principles of CMOS VLSI Design". 2<sup>nd</sup> Edition. Addison-Wesley, 2000.
2. Douglas a. Pucknell and K. Eshragian., "Basic VLSI Design" 3<sup>rd</sup> Edition. PHI, 2000.
3. R. Jacob Baker, Harry W. LL., & David K. Boyce., "CMOS Circuit Design", 3<sup>rd</sup> Indian reprint, PHI, 2000.

### **REFERENCE BOOKS:**

1. Semiconductor Devices Modelling and Technology Nandita Das Guptha , Amitava Das Guptha; Prentice Hall India
2. Operation and Modeling of The MOS transistor : Yannistividis 2/e Oxford University Press
3. Kang &Leblebigi "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003
4. Weste and Eshraghian, "Principles of CMOS VLSI design" Addison-Wesley, 2002

## COURSE PLAN

<b>08 EC 6321CMOS VLSI Design(L-T-P : 4-0-0) CREDITS:4</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, MOS Transistor Theory - Introduction MOS Device Design Equations,	<b>8</b>	<b>15</b>
<b>MODULE : 2</b> The Complementary CMOS Inverter-DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, The Tri State Inverter, Bipolar Devices, Resistance Estimation Capacitance Estimation, Inductance, Switching Characteristics CMOS-Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margining, Reliability.	<b>8</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> CMOS Logic Gate Design, Basic Physical Design of Simple Gate, CMOS Logic Structures, Clocking Strategies, I/O Structures, Low Power Design	<b>8</b>	<b>15</b>
<b>MODULE : 4</b> Design Strategies CMOS Chip Design Options, Design Methods, Design Capture Tools, Design Verification Tools, Design Economics, Data Sheets,	<b>8</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> CMOS Testing -Manufacturing Test Principles, Design Strategies for Test, Chip Level Test Techniques, System Level Test Techniques, Layout Design for Improved Testability.	<b>10</b>	<b>20</b>
<b>MODULE : 6</b> Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.	<b>10</b>	<b>20</b>

## 08 EC 6331ADVANCED DIGITAL SYSTEM DESIGN

Pre-requisites: Nil

Credits: 3-0-0: 3  
Year: 2015

### Course Objectives:

- A foundation in fundamental of sequential circuits
- Practice in designing sequential circuits-mealy ,moore and FM charts
- An introduction to VHDL basing

### Syllabus

Design of multiple output sequential circuits, introduction to PLDS, state diagram, state table minimization of mealy and moor machine, Race conditions and cycles, Hazards, FM charts, Different modeling in VHDL, Model simulation, Synthesis –Issues, Timing simulation

### Course Outcome:

After completion of this course students are able to design-sequential circuits, multiple output combination circuits & SM charts..Also to write VHDL programs & simulate

### Text Books: One or two text books only (if required)

1. “Fundamentals of Digital Design”, Charles H.Roth, Jr., PWS Pub.Co., 1998.
2. “Digital Design Fundamentals”, Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New Jersey.1989.

### References:

1. Kevin Skahill, "VHDL for Programmable Logic", Addison -Wesley, 1996
2. Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGRAW-Hill, 1998

## COURSE PLAN

<b>08 EC 6331Advanced Digital System Design (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Introduction - Design of Combinational Systems - Multiple output combination circuit design - McCluskey method- Introduction to PLDs - PROM based design - PAL - Arithmetic PAL devices - Study based on PAL22V10, CPLDs (MAX3000A CPLD).	<b>6</b>	<b>15</b>
<b>MODULE:2</b> Mealy Machine, Moore Machine, State diagrams, State table minimization, Incompletely specified sequential machine	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Asynchronous sequential circuit design (fundamental mode), Derivation of excitation table, Designing with SM charts - State machine charts, Derivation of SM charts, and Realization of SM charts.	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Hazards, Race conditions and cycles, Static and dynamic hazards, Methods for avoiding races and hazards, essential hazards	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Introduction to HDL - Behavioral modeling - Data flow modeling- Structural modeling- Basic language elements - Entity-Architecture- Configurations - Subprograms and operator overloading- Packages and libraries	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> VHDL advanced features - Model simulation - Hardware modeling examples. Synthesis. Timing Simulation. VHDL Synthesis Issues.	<b>8</b>	<b>20</b>

## 08 EC 6341VLSI FABRICATION TECHNOLOGY

Pre-requisites: Nil

Credits: 3-0-0: 3

Year: 2015

### Course Objectives:

- To make students know various steps involved in VLSI fabrication.
- To make students aware of various IC technologies and packaging of VLSI devices.

### Syllabus:

Crystal Growth and Wafer Preparation- Epitaxy, Lithography, Reactive Plasma Etching, Dielectric and Polysilicon Film Deposition, Ion Implantation, Metallization; VLSI Process Integration; Packaging of VLSI Devices.

### Course Outcome:

Students who successfully complete this course will be aware of the manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI chip fabrication; different IC technologies and fabrication; VLSI device packaging and design considerations

#### TEXT BOOKS:

1. S. M. Sze, "VLSI Technology", McGraw-Hill, Second Edition.
2. S.K. Ghandhi, "VLSI Fabrication Principles", John Wiley Inc., New York, 1994, Second Edition.
3. S.A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 2nd edition, 2001

#### REFERENCE BOOKS:

1. S. Wolf and R. Tauber, "Silicon Processing for the VLSI Era", Lattice Press, 1986.
2. Plummer, Deal and Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall, July 2000.

## COURSE PLAN

<b>08 EC 6341VLSI Fabrication Technology (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Introduction, Electronic-Grade Silicon, Czochralski Crystal Growing, Silicon Shaping, Process Considerations <b>Epitaxy:</b> Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation.	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Introduction, Optical Lithography, Electron Lithography, X-ray Lithography, Ion Lithography. Optical contrast,contrastcurve,MTF	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Reactive Plasma Etching: Introduction, Plasma Properties, Feature-Size Control and Anisotropic Etch Mechanisms, Other Properties of Etch Processes, Reactive Plasma-Etching Techniques and Equipment, Specific Etch Processes,P-well,N-well,twin-well process	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Ion Implantation:Introduction, Range Theory, Implantation Equipment, Annealing, Shallow Junctions, High-Energy Implantation, isolation methods-PN junction, Trench isolation,ohmic contacts	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Metallization: Introduction, Metallization Applications, Metallization Choices, Physical Vapor Deposition, Patterning, Metallization Problems, New Role of Metallization, Testing of VLSI circuits	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, , CMOS IC Technology,, Bipolar IC Technology, IC Fabrication, Stick diagram-rules for stick diagram, design rules Packaging of VLSI Devices: Introduction, Package Types, Packaging Design Considerations	<b>8</b>	<b>20</b>



## 08 EC 6351(A): ELECTRONIC SYSTEM DESIGN

Pre-requisites: Nil

Credits: 3-0-0: 3  
Year: 2015

### Course Objectives:

- To make students to practical circuits design issues and techniques
- To make students aware of various filtering systems, electrostatic discharges etc

### Syllabus:

Practical analog and mixed signal circuit design issues and techniques, practical logic circuit design and issues, Electromagnetic compatibility, Balancing & Filtering in Electronic Systems, Protection against Electrostatic Discharges (ESD), Packaging & Enclosures of Electronic System, Cooling in/of Electronic System

### Course Outcome:

Students who successfully complete this course will be able to Practical analog and mixed signal circuit design issues and techniques, practical logic circuit design and issues

### TEXT BOOKS:

1. Electronic Instrument Design, 1st edition; by: Kim R. Fowler; Oxford University Press.
2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W. Ott John Wiley & Sons.
3. Digital Design Principles & Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.
4. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc
5. Intuitive Analog circuit design by: Mark. T Thompson; Published by Elsevier

### REFERENCE BOOKS:

1. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.
2. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ <http://www.analog.com>
3. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539@ <http://www.analog.com>

## COURSE PLAN

<b>08 EC 6351(A) : ELECTRONIC SYSTEM DESIGN(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<p><b>MODULE : 1</b>            Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components,. Op amps: DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier</p>	<b>6</b>	<b>15</b>
<p><b>MODULE : 2</b>            Design issues affecting dc accuracy &amp; error budget analysis in instrumentation amplifier applications. Isolation amplifier basics. Active filters: design of low pass, high pass and band pass filters. ADCs and DACs: Characteristics, interfacing to microcontrollers. Selecting an ADC. Power supplies: Characteristics, design of full wave bridge regulated power supply. Circuit layout and grounding in mixed signal system.</p>	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<p><b>MODULE : 3</b>  <b>Practical Logic Circuit Design Issues and Techniques:</b> Understanding and interpreting data sheets &amp; specifications of various CMOS&amp;BiCMOS family Logic devices. Electrical behavior (steady state &amp; dynamic) of CMOS &amp;BiCMOS family logic devices. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies. CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations</p>	<b>6</b>	<b>15</b>
<p><b>MODULE : 4</b>            Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI. Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems. Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables</p>	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		

<p><b>MODULE : 5</b> Grounding of Electronic Systems: Safety grounds, signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies. Balancing &amp; Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, and system bandwidth.</p>	7	20
<p><b>MODULE : 6</b>  Protection Against Electrostatic Discharges (ESD):Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC.Packaging&amp; Enclosures of Electronic System: Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging's influence and its factors. Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.</p>	8	20

## **08 EC 6351(B): DIGITAL INTEGRATED CIRCUIT DESIGN**

**Credits: 3-0-0: 3**

**Pre-requisites: Nil**

**Year: 2015**

### **Course Objectives:**

- To make students to idea about digital integrated circuits
- To make students aware of CMOS logics, arithmetic circuits using CMOS

### **Syllabus:**

CMOS inverters, Static CMOS design combinational and sequential circuits, Arithmetic circuits in CMOS VLSI, Bipolar gate design

### **Course Outcome:**

Students who successfully complete this course will be able to idea about Basic CMOS circuits in VLSI, and to design integrated circuits using CMOS logic

### **TEXT BOOKS:**

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, MGH, Second Ed., 1999
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, 1997
3. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 2000
4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout and simulation. New York: IEEE Press, 1998.
5. Analysis and Design of Digital Integrated Circuits, Third Edition, David A. Hodges, Horace G. Jackson, and Resve A. Saleh, McGraw-Hill, 2004.

## COURSE PLAN

<b>08 EC 6351(B) DIGITAL INTEGRATED CIRCUIT DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> CMOS inverters -static and dynamic characteristics, CMOS NAND, NOR and XOR Gates. Calculation or delay times of CMOS Inverter	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Static CMOS design combinational and sequential circuits -Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> CMOS transmission gates-Simple circuit using TG-basic principle of pass transistor logic-Voltage bootstrapping-CMOS ring oscillator	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Dynamic CMOS logic-Precharge/ evaluable logic-cascading problem-domino logic-cascading domino logic gates-Charge sharing in domino logic-realisation of simple functions using domino logic-NORA logic-True single phase clock dynamic logic	<b>8</b>	<b>20</b>

## **08 EC 6351(C): DESIGNING WITH MICROCONTROLLERS**

**Pre-requisites: Nil**

**Credits: 3-0-0: 3**

**Year: 2015**

### **Course Objectives:**

- To make students know about 8051 microcontrollers.
- To make students aware of various ARM processors

### **Syllabus:**

18-Bit 8051 Microcontroller, 32- Bit ARM920T Processor Core Introduction, Programmers Model, Cache, memory management, ARM instruction set, ARM 9 microcontroller architecture

### **Course Outcome:**

Students who successfully complete this course will be able to know about 18 bit microcontrollers and different ARM processors

### **TEXT BOOKS:**

1. Intel Hand Book on “Embedded Microcontrollers”, 1st Edition
2. Muhammad Ali Mazidi, Janice GillispieMazidi, Rolin D. McKinlay, “The 8051 Microcontroller and Embedded Systems using Assembly and C”, 2nd Edition, Prentice Hall
3. ARM Company Ltd. “ARM Architecture Reference Manual– ARM DDI 0100E”
4. David Seal “ARM Architecture Reference Manual”, 2001 Addison Wesley, England; Morgan Kaufmann Publishers

### **REFERENCE BOOKS:**

1. Ayala, Kenneth J “8051 Microcontroller - Architecture, Programming & Applications”, 1st Edition, Penram International Publishing
2. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
3. Predko, Myke, “Programming and Customizing the 8051 Microcontroller”, 1<sup>st</sup> Edition, McGraw Hill International

## COURSE PLAN

<b>08 EC 6351(C): DESIGNING WITH MICROCONTROLLERS (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<p><b>MODULE 1:</b> 18-Bit 8051 Microcontroller: Introduction to Embedded Systems.8-Bit Microcontrollers: A popular 8-bit Microcontroller (Intel 8051) is covered under this section Architecture: CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts Peripherals: Timers, Serial Port, I/O Port Programming: Addressing Modes, Instruction Set, Programming Microcontroller based System Design: Timing Analysis, Case study with reference to 8-bit 8051 Microcontroller. A typical application design from requirement analysis through concept design, detailed hardware and software design using 8-bit 8051 Microcontrollers.</p>	<b>6</b>	<b>15</b>
<p><b>MODULE : 2</b> 32- Bit ARM920T Processor Core Introduction:RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram Programmers Model: Data Types, Processor modes, Registers, General Purpose Registers, Program Status Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table, Architecture revisions, ARM Processor Families.Cache:Memory hierarchy and cache memory, Cache Architecture – Basic Architecture of a Cache, Basic operation of a cache controller, Cache and main memory relationship, Set Associativity Cache Policy – Write policy, Cache line replacement policies, allocation policy on a cache miss Instruction Cache, Data Cache, Write Buffer and Physical Address TAG RAM</p>	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<p><b>MODULE:3</b> Memory Management Units: How virtual memory works, Details of the ARM MMU, Page Tables, Translation Look-aside Buffer, Domains and Memory access permissions ARM Instruction Set: Data Processing instructions, Branch instructions, Load - Store instructions, Software Interrupt Instruction, Program Status Register Instruction, Loading Constants Thumb Instruction Set: Thumb register usage, ARM-Thumb interworking, Branch instruction, Data processing instructions, Load - store instructions, stack instructions, software interrupt instructions. Interrupt Handling: Interrupts, Assigning interrupts, Interrupt latency, IRQ &amp; FIQ exceptions, Basic interrupt stack design and implementation, Non-nested Interrupt handle</p>	<b>6</b>	<b>15</b>
<p><b>MODULE : 4</b> ARM9 Microcontroller Architecture: A popular ARM9 Microcontroller from Atmel (AT91RM9200) is covered under this sectionAT91RM9200 Architecture: Block Diagram, Features, Memory Mapping Memory Controller (MC), Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping</p>	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		

<p><b>MODULE : 5</b>  External Bus Interface (EBI), Organization of the External Bus Interface, EBI Connections to Memory Devices External Memory Interface, Write Access, Read Access, Wait State Management  <b>AT91RM9200 PERIPHERALS</b> Interrupt Controller: Normal Interrupt, Fast Interrupt, AIC System Timer (ST):Period Interval Timer (PIT), Watchdog Timer (WDT), Real time Timer (RTT)Real Time Clock (RTC), Parallel Input/output Controller (PIO)</p>	<b>7</b>	<b>20</b>
<p><b>MODULE : 6</b>  <b>AT91RM9200 PERIPHERALS:</b> Universal Synchronous Asynchronous Receiver Transceiver (USART):Block Diagram, Functional Description, Synchronous and Asynchronous Modes Development  &amp; Debugging Tools for Microcontroller based Embedded Systems: Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc. Brief Architecture of Power PC.</p>	<b>8</b>	<b>20</b>



## 08GN6001: RESEARCH METHODOLOGY

Credits:0-2-0:2

### Course Objectives

The main objective of the course is to provide a familiarization with research methodology and to induct the student into the overall research process and methodologies. This course addresses: The scientific research process and the various steps involved formulation of research problem and research design, design of experiments, thesis preparation and presentation, research proposals, publications and ethics; Important research methods in engineering. As a tutorial type course, this course is expected to be more learner centric and active involvement from the learners are expected which encourages self-study and group discussions. The faculty mainly performs a facilitator's role.

### Syllabus

Overview of research methodology - research process - scientific methods - research problem and design - research design process - formulation of research task, literature review and web as a source - problem solving approaches - experimental research - ex post facto research. Thesis writing - reporting and presentation - interpretation and report writing - principles of thesis writing- format of reporting, oral presentation - seminars and conferences

Research proposals - research paper writing - publications and ethics - considerations in publishing, citation, plagiarism and intellectual property rights. Research methods - modelling and simulation - mathematical modeling - graphs - heuristic optimization - simulation modeling - measurement design - validity - reliability - scaling - sample design - data collection methods and data analysis

### Course Outcome

At the end of course, the student will be able to:

Discuss research methodology concepts, research problems, research designs, thesis preparations, publications and research methods.

Analyze and evaluate research works and to formulate a research problem to pursue research

Prepare a thesis or a technical paper, and present or publish them

Apply the various research methods followed in engineering research for formulation and design of own research problems and to utilize them in their research project.

### Reference:

1. C. R. Kothari, (2004) "*Research Methodology, Methods and Techniques*", New Age International Publishers
2. R. Panneerselvam,(2014) "*Research Methodology*", PHI Learning
3. K. N. Krishnaswamy, Appa Iyer Sivakumar, M. Mathirajan, (2006) ) "*Management Research Methodology, Integration of principles, Methods and Techniques*, Pearson Education

4. Deepak Chawla, Meena Sondhi,(2011) "*Research Methodology – concepts & cases*", Vikas Publishing House
5. J.W. Bames, "*Statistical Analysis for Engineers and Scientists*", McGraw Hill, New York
6. . Schank Fr.,(2008) "*Theories of Engineering Experiments*", Tata Mc Graw Hill Publication.
7. John W Best, James V Kahan, (2010) "*Research in Education*", PHI Learning
8. Sinha, S. C. and Dhiman, A. K. (2002), "*Research Methodology*", ESS Publications. (2 volumes)

<b>08 GN6001: RESEARCH METHODOLOGY (L-T-P : 0-2-0) CREDITS:2</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE: 1</b> <b>Overview of Research Methodology:</b> Research concepts – meaning – objectives – motivation - types of research –research process – criteria for good research – problems encountered by Indian researchers - scientific method - research design process	<b>5</b>	<b>15</b>
<b>MODULE: 2</b> <b>Research Problem and Design:</b> Formulation of research task – literature review – methods – primary and secondary sources – web as a source – browsing tools - formulation of research problems – exploration - hypothesis generation - problem solving approaches –Concepts of introduction To TRIZ-experimental research – principles – Laboratory experiment - experimental designs - ex post facto research-qualitative research	<b>5</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE: 3</b> <b>Thesis writing, reporting and presentation:</b> significance of report writing— principles of thesis writing- different steps in report writing Interpretation in writing – techniques of interpretation – precautions in interpretation - format of reporting - – layout and mechanics of research report -references – tables – figures – conclusions – oral presentation – preparation – making presentation – use of visual aids - effective communication - preparation for and presentation in seminars and conferences	<b>4</b>	<b>15</b>
<b>MODULE: 4</b> <b>Research proposals, publications, ethics and IPR:</b> Research proposals - development and evaluation –research paper writing – layout of a research paper - journals in engineering – considerations in publishing –concept of impact factor– citations - open access publication - ethical issues -plagiarism – software for plagiarism checking intellectual property right- patenting case studies .	<b>5</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE: 5</b> <b>Research methods – Modelling and Simulation:</b> Modelling and Simulation – concepts of modelling –mathematical modelling - composite modelling –modelling	<b>5</b>	<b>20</b>

with – ordinary differential equations – partial differential equations – graphs- heuristics and heuristic optimization - simulation modeling		
<b>MODULE: 6</b> <b>Research Methods – Measurement, sampling and Data acquisition:</b> Measurement design – errors -validity and reliability in measurement - scaling and scale construction - sample design - sample size determination - sampling errors - data collection procedures - sources of data – data collection methods - data preparation and data analysis	<b>4</b>	<b>20</b>

### 08 EC 6371: SEMINAR

**Pre-requisites: Nil**

**Credits: 0-0-0: 2**  
**Year: 2015**

Objective: To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self-esteem and courage that are essential for engineers.

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

**08 EC 6381: VLSI DESIGN LAB****(L-T-P: 0-0-2) CREDITS: 2****COURSE PLAN**

<b>08 EC 6381: :VLSI Design lab (L-T-P : 0-0-2) CREDITS:2</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> 1. Modeling and simulation of Combinational and sequential circuits using Verilog/VHDL. 2. Modeling and Simulation of ALU using Verilog/VHDL. 3. Modeling and Simulation of FSMs using Verilog/VHDL 4. Modeling and simulation of Memory and FIFO in Verilog/VHDL 5. Modeling and simulation of UART in Verilog/VHDL	<b>13</b>	<b>50</b>
<b>MODULE : 2</b> 1.Implementing the designs n module 1 on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits 2. Simulation of NMOS and CMOS circuits. 3. Modelling of MOSFET.	<b>13</b>	<b>50</b>

## **SEMESTER 2**

### **08 EC 6312 ANALOG VLSI DESIGN**

**Credits: 3-0-0: 3**

**Year: 2015**

**Pre-requisites: Nil**

#### **Course Objectives:**

- A foundation in the fundamentals of Analog VLSI Design;
- Ability to design of IC MOS Amplifiers and PLL
- An introduction to challenges facing in Analog IC Design;

#### **Syllabus**

Fundamental concepts and overview; Analog MOS Models ; Active and Passive device fabrication; Basics of single stage CMOS amplifiers; CMOS Differential Amplifiers; Design of single and two stage CMOS Op-amps ; High frequency Op-amps; Design of non-linear and wave shaping circuits ; Switched capacitor circuits; Design of DPLL and DLL; Basics of CMOS data converters.

#### **Course Outcome:**

Students who successfully complete this course will have demonstrated an ability to apply the fundamental concepts of Analog VLSI Design; ability to design IC MOS Amplifiers; ability to design DPLL which is used in various fields. Students will be familiarized with the challenges in Analog IC design.

**Text Books:** One or two text books only ( if required)

1. "Analog Integrated Circuit Design", David. A. Johns and Ken Martin, John Wiley and Sons, 2001.
2. "Design of Analog CMOS Integrated Circuit", BehzadRazavi, Tata McGraw HILL, 2002.
3. "CMOS Analog Circuit Design", Philip Allen & Douglas Holberg, Oxford University Press, 2002.

#### **References:**

"Analog VLSI – Signal Information and Processing", Mohammed Ismail &Feiz , John Wiley and Sons.

## COURSE PLAN

<b>08 EC 6312 ANALOG VLSI DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Analog MOS transistor models Temperature effects and Noise in MOS transistor MOS resistors, characterization of resistive, capacitive elements and MOS devices	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Passive and active CMOS current sink/ sources– basics of single stage CMOS amplifiers common Source, common gate and source follower stages frequency response.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> CMOS Differential Amplifiers: CMOS Operational Amplifiers one stage and two stage gain boosting Common mode feedback (CMFB) Cascode and Folded cascade structures	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> High Performance Opamps – High speed/ high frequency opamps, micro power opamps, low noise opamps and low voltage opamps. Current mirrors, filter implementations	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Supply independent and temperature independent references Band gap references PTAT current generation and constant Gm biasing – CMOS comparators – Multipliers and wave shaping circuits – effects due to nonlinearity and mismatch in MOS circuits. Switched Capacitor Circuits: First and Second Order Switched Capacitor Circuits,	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Switched Capacitor filters, CMOS oscillators, simple and charge pump CMOS PLLs non ideal effects in PLLs, Delay locked loops and applications, basics of CMOS data converters – Medium and high speed CMOS data converters, Over sampling converters.	<b>8</b>	<b>20</b>

## 08 EC 6322 CAD OF VLSI CIRCUITS

**Pre-requisites:** Nil

**Credits:** 3-0-0: 3

**Year:** 2015

### **Course Objectives:**

- This objective is to provide the idea about various CAD tools front end back end design

### **Syllabus**

Fundamental concepts and overview; Various CAD Tools for front end and Back end design, Introduction to VLSI Methodologies, Introduction to Design Tools, Layout Algorithms Circuit partitioning, Dataflow modeling

### **Course Outcome:**

Students who successfully complete this course will have demonstrated an ability to apply the fundamental concepts of CAD of VLSI circuits.

### **Text Books:**

1. N.A. Sherwani, " Algorithms for VLSI Physical Design Automation ", 1999.
2. S.H. Gerez, " Algorithms for VLSI Design Automation ", 1998.4. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992
3. Drechsler, R., *Evolutionary Algorithms for VLSI CAD*, Kluwer Academic Publishers, Boston, 1998.
4. Verilog HDL by Samir Palnitkar

## COURSE PLAN

<b>08 EC 6322 CAD of VLSI Circuits(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Various CAD Tools for front end and Back end design, Schematic editors, Layout editors, Place and Route tools	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Introduction to VLSI Methodologies - VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Introduction to Design Tools: Introduction & Familiarity with Design Tools from various vendors e.g. Synopsis, Mentor Tools etc. Verilog Basics - Modeling Levels - Data Types - Modules and Ports - Instances - Basic Language Concepts	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Dataflow modelling – Behavioural modeling Modelling and Simulation of systems/subsystems using Verilog HDL. Typical case studies.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 5</b> Layout Algorithms Circuit partitioning, placement, and routing algorithms; Design rule verification; Circuit Compaction; Circuit extraction and post-layout simulation	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Automatic Test Program Generation; Combinational testing D-Algorithm and PODEM algorithm; Scan-based testing of sequential circuits; Testability measures for circuits.	<b>8</b>	<b>20</b>



# 08 EC 6332 TESTING AND VERIFICATION OF VLSI CIRCUITS

Credits: 3-0-0: 3

Year: 2015

Pre-requisites: Nil

## Course Objectives:

- To study the issues in testing; understand the fundamentals of VLSI and system testing with fault models and simulation
- To explore the concept in boundary scan, BIST for logic and memories with simple intellectual property of core based design in SoC

## Syllabus

Scope and issues in testing and verification of ic,s-introduction to test benches and verilog test bench code unity-various fault models-boundary scan-ATPG-BIST-simple IP's design for memory and core RISC CPU design

## Course Outcome:

- Upon completion of the course with laboratory practice.
- Students will obtain the skill in writing test bench coding for combinational, sequential circuits
- Able to analyze and identify simple fault models to combinational and sequential circuits

## Text Books:

1. M. Abramovici, M. A. Breuer, A. D. Friedman, "Digital Systems Testing and Testable Design" Piscataway, New Jersey: IEEE Press, 1994
2. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000
3. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
4. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
5. Samiha Mourad and Yervant Zorian, "Principles of Testing Electronic Systems", Wiley (2000).

## REFERENCES

1. "SoC Verification Methodology and Techniques", Prakash Rashinkar Peter Paterson and Leena Singh .Kluwer Academic Publishers, 2001.
2. "Reuse Methodology manual for System On A Chip Designs", Michael Keating,

## COURSE PLAN

<b>08 EC 6332 TESTING AND VERIFICATION OF VLSI CIRCUITS (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
MODULE : 1 <b>Introduction:</b> Scope of testing and verification in VLSI design process; Issues in testand verification of complex chips, embedded cores and SOCs, Fault models	<b>6</b>	<b>15</b>
MODULE : 2 Test coding: Introduction to test benches, writing test benches in Verilog HDL.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
MODULE : 3 Fundamentals of VLSI testing, Automatic test pattern generation, Design for testability	<b>6</b>	<b>15</b>
MODULE : 4 Scan design: Test interface and boundary scan	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
MODULE : 5 System Testing and test for SOCs, Iddq testing, Delay fault testing, BIST for testing of logic and memories, Test automation.	<b>7</b>	<b>20</b>
MODULE : 6 Design Verification Techniques based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking. Verification of simple IPs: Memory verification, FIFO verification and Verification of RISC CPU	<b>8</b>	<b>20</b>

## 08 EC 6342(A)LOW POWER VLSI DESIGN

Credits: 3-0-0: 3

Year: 2015

Pre-requisites: Nil

### Course Objectives:

- skills to effectively apply analytical and simulation techniques for power analysis of CMOS VLSI
- Utilize probabilistic analysis

### Syllabus

Probabilistic Power Analysis, Circuit –Transistor and Gate Sizing, Equivalent Pin Ordering, Advanced Techniques –Adiabatic Computation, Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits. Low Power Static RAM Architectures -Low Energy Computing

### Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze the requirements of low power CMOS VLSI design
- Applying effective simulation techniques for power analysis
- Optimizing power at various levels of design abstraction
- Constructing low energy computing system

### Text Books:

1. Gary Yeap" Practical Low Power Digital VLSI Design ", 1997.
2. Kaushik Roy, Sharat Prasad, " Low Power CMOS VLSI Circuit Design ", 20003.  
A.P.Chandrakasan and R.W. Broadersen, Low power digital CMOS design, Kluwer,1995

### REFERENCE BOOKS:

1. CMOS Analog Circuit Design", Philip Allen & Douglas Holberg, Oxford University Press, 2002.
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

## COURSE PLAN

<b>08 EC 6342(A)LOW POWER VLSI DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Introduction –Charging and Discharging of Capacitance, Short Circuit Current in CMOS Circuits, CMOS Leakage Current, Static Current, Basic Principles of Low Power Design, Low Power Figure of Merits. Simulation Power Analysis-SPICE Circuit Simulation, Gate Level Logic Simulation, Architecture Level Analysis, Data Correlation Analysis, Monte Carlo Simulation.	<b>6</b>	<b>15</b>
<b>MODULE:2</b> Probabilistic Power Analysis- Random Logic Signals, Static Probability, Transition Density, Techniques of Power Analysis, Gate Level Power Analysis, Power Estimation using Entropy-Combinational logic systems, Sequential logic systems.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
Circuit –Transistor and Gate Sizing, Equivalent Pin Ordering, network Restructuring and Reorganization, Special Latches and Flip Flops, Low Power Digital Cell Library, Logic –Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre-computation Logic. Special Techniques –Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Low Power Techniques for SRAM, Architecture and Systems-Power and Performance Management, Switching Activity Reduction, Parallel Architecture with Voltage Reduction.	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Advanced Techniques –Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuits, Reversible Logic Circuits, Elimination of Garbage outputs	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Physics of Power Dissipation in CMOS FET Devices- MIS Structure, Energy band representations, Threshold Voltage, Surface Space Charge Region, Threshold Voltage, Depletion Region Analysis- Depth of Depletion Region, Inversion Layer thickness, Charge in Inversion Layer, Long Channel MOSFET- Body Effect, Sub-threshold Current, Sub-threshold Swing.	<b>7</b>	<b>20</b>

<p>MODULE : 6  Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits. Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques – Software Design for Low Power.</p>	<b>8</b>	<b>20</b>
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## **08 EC 6342 (B) SYNTHESSES AND OPTIMIZATION OF DIGITAL CIRCUITS**

**Pre-requisites: Nil**

**Credits: 3-0-0: 3**

**Year: 2015**

### **Course Objectives:**

- To study detail in detail about different digital circuits and various optimization techniques
- To analyze embedded system design along with different perspectives

### **Syllabus**

Introduction to synthesis and optimization, Logic synthesis, Optimization of digital circuits introduction to hardware and software co design

### **Course Outcome:**

On successful completion of this subject, the student should be capable of

- Analyze the software and hardware co-design
- Analyze the optimization of digital circuits

### **Text Books:**

1. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw-Hill, 1994, 5th print.
2. "Logic Synthesis", S. Devadas, A. Ghosh and K. Keutzer, McGraw Hill, 1994.
3. R. Gupta, "Co-synthesis of Hardware and Software for Embedded Systems", Kluwer 1995.

### **REFERENCE BOOKS:**

1. Edwards M.D., *Automatic Logic synthesis Techniques for Digital Systems*, Macmillan New Electronic Series, 1992
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education

## COURSE PLAN

<b>08 EC 6342(B) SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Introduction to Synthesis and optimization: High-level synthesis: Motivation and organization, Scheduling Resource sharing, Data path and control synthesis	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Logic synthesis: Algorithms and rule-based systems, Algebraic and Boolean methods	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Timing issues: Sequential synthesis and retiming, Semicustom libraries & library mapping, Algorithms and rule-based systems, Structural and Boolean matching	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Optimization of digital circuits: Area, Timing and power optimization. RTL Coding for area, timing and power optimization.	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Synthesis and Generation of area, timing and power reports: RISC CPU a case study.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Introduction to Hw/Sw Co-design, Problem taxonomy, Embedded system design, Software optimization, Perspectives	<b>8</b>	<b>20</b>

# 08 EC 6342(C)DESIGN OF DIGITAL SIGNAL PROCESSING

Credits: 3-0-0: 3

Pre-requisites: Nil

Year: 2015

## Course Objectives:

- To study detail in detail about digital signal processors
- Make a knowledge about current trends in digital signal processors

## Syllabus

Digital signal processor, algorithms, applications and current trends in digital signal processors

## Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze the Digital signal processors
- Analyze the applications and current trends

## Text Books:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1<sup>st</sup> Edition; by: NaimDahnoun
2. DSP Applications using 'C' and the TMS320C6X DSK, 1<sup>st</sup> Edition; by: RulphChassaing
3. Digital Signal Processing: A System Design Approach, 1<sup>st</sup> Edition; by: David J Defatta J, Lucas Joseph G &Hodkiss William S; John Wiley
4. Digital Signal Processing with Field Programmable Gate Arrays: 2<sup>nd</sup> Edition, by: U. Meyer – Base, Springer
5. Real - Time Digital Signal Processing: Implementations, Applications, and Experiments with the TMS320C55X, Kuo, Sen M, Lee, Bob H, John Wiley & Sons Ltd.

## REFERENCE BOOKS:

1. Digital Signal Processing, Third Edition, Sanjit K. Mitra, Tata McGRWA Hill
2. Digital Signal Processing – A Practical Guide for Engineers and Scientists, Steven W Smith, Elsevier

## COURSE PLAN

<b>08 EC 6342(C) DESIGN OF DIGITAL SIGNAL PROCESSING (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<p>MODULE : 1</p> <p><b>Digital Signal Processor:</b> TMS320C6713 or any other popular DSP from Texas Instruments is covered under this module Architecture: CPU Architecture, Internal Memory, CPU Data Paths control Programming: Instruction Set and Addressing Modes</p>	<b>6</b>	<b>15</b>
<p>MODULE : 2</p> <p>Code Composer Studio, Code Generation Tools, Code Composer Studio Debug Tools DSP Peripherals: Multichannel Buffered Serial Port, Transmission &amp; Reception Timers Memory of DSP: Internal Data/Program Memory External Memory Interface</p>	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<p>MODULE : 3</p> <p><b>Digital Signal Processing Algorithms:</b> Filter Design: FIR Digital filter design. Fourier Transform: DFT, FFT, Spectral Analysis,DTMF Speech Processing Algorithms</p>	<b>6</b>	<b>15</b>
<p>MODULE : 4</p> <p>Real-time Implementation: Implementation of Real-time FIR Digital filter using DSP.Implementation of Real-time Fast Fourier Transform applications using the DSP Implementation of DTMF Tone Generation and Detection. Implementation of Speech processing applications</p>	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<p>MODULE :5</p> <p><b>Current trends in Digital Signal Processor:</b> FPGA Technology, DSP Technology Requirements, Design implementation, Multiply Accumulator (MAC) and Sum of Product (SOP), Implementation of Serial/Parallel Convolver using FPGAs,FPGA Based DSP System Design</p>	<b>7</b>	<b>20</b>
<p>MODULE : 6</p> <p>FIR filters, FIR Theory, Designing FIR filters, Direct Window Design method, Constant Coefficient FIR Design, Direct FIR Design, Cooley-Tukey FFT Algorithm implementation using FPGA</p>	<b>8</b>	<b>20</b>



# 08 EC 6352(A) HIGH SPEED DIGITAL DESIGN

Credits: 3-0-0: 3

Year: 2015

Pre-requisites: Nil

## Course Objectives:

- To study detail in high speed digital circuits
- Power distribution and noise in high speed digital circuits

## Syllabus

Introduction to high speed digital design, Power distribution and noise, Signalling convention and circuits, Timing convention and synchronizations

## Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze the basic idea of high speed digital design
- Analyze the power distribution and noise

## Text Books:

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic", 3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " System Design", Wiley , 2007
3. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006
4. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

## REFERENCE BOOKS:

1. William S. Dally & John W. Poulton; Digital Systems Engineering, Cambridge University Press, 1998
2. Masakazu Shoji; High Speed Digital Circuits, Addison Wesley Publishing Company, 1996
3. Jan M, Rabaey, et all; Digital Integrated Circuits: A Design perspective, Second Edition, 2003

## COURSE PLAN

<b>08 EC 6352(A) HIGH SPEED DIGITAL DESIGN(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Frequency, time and distance - Capacitance and inductance effects - High speed properties of logic gates - Speed and power	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Modelling of wires -Geometry and electrical properties of wires - Electrical models of wires - transmission lines - lossless LC transmission lines - lossy LRC transmission lines - special transmission lines	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Power supply network - local power regulation - IR drops - area bonding - onchip bypass capacitors - symbiotic bypass capacitors - power supply isolation	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Noise sources in digital system - power supply noise - cross talk – inter symbol interference. <b>Signalling convention and circuits</b> -Signalling modes for transmission lines -signalling over lumped transmission media	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> signalling over RC interconnect - driving lossy LC lines - simultaneous bi-directional signalling - terminations - transmitter and receiver circuits- <b>Timing convention and synchronisation</b> -Timing fundamentals - timing properties of clocked storage elements	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - synchronization failure and meta stability - PLL and D LL based clock aligners	<b>8</b>	<b>20</b>

# 08 EC 6352(B) SOC DESIGN AND VERIFICATION

**Pre-requisites:** Nil

**Credits:** 3-0-0: 3

**Year:** 2015

## **Course Objectives:**

- To familiarize the design of SoC process using few techniques and verify the issues regarding that and also to design the communication architecture for SoC's
- Power distribution and noise in high speed digital circuits

## **Syllabus**

Introduction to system on chip design process, Marco design process, SoC verification, Design of communication architecture of SoC's

## **Course Outcome:**

On successful completion of this subject, the student should be capable of

- Analyze the SoC design process
- Analyze the design of communication architecture for SoC's

## **Text Books:**

1. "SoC Verification Methodology and Techniques", Prakash Rashinkar Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.
2. "Reuse Methodology manual for System On A Chip Designs", Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001.

## COURSE PLAN

<b>08 EC 6352(B) SOC DESIGN AND VERIFICATION (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE 1 :</b> <b>System On Chip Design Process:</b> A canonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> System Design process, System level design issues, Soft IP Vs Hard IP, Design for timing closure, Logic design issues Verification strategy, On chip buses and interfaces, Low Power, Manufacturing test strategies.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE:3</b> <b>Macro Design Process:</b> Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design, System Integration wit reusable macros.	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> <b>SoC Verification:</b> Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans.	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> System level verification, Block level verification, Hardware/software co verification and Static net list verification. Verification architecture, Verification components, Introduction to VMM, OVM and UVM.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> <b>Design of Communication Architectures For SoCs:</b> On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures, Communication architecture tuners, Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.	<b>8</b>	<b>20</b>

## 08 EC 6352(C) NANO ELECTRONICS

**Pre-requisites:** Nil

**Credits:** 3-0-0: 3  
**Year:** 2015

### **Course Objectives:**

- To impart the idea of nano electronics technology in detail for the application of devices

### **Syllabus**

Introduction to nano-electronics, Characterization, in organic semiconductor nanostructures, Fabrication techniques, physical processes. Methods of measuring properties structure, Applications

### **Course Outcome:**

On successful completion of this subject, the student should be capable of

- Analyze the fundamentals of nano electronics
- Analyze the methods of measuring structures

### **Text Books:**

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale science and technology", John Wiley and sons, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, copyright 2006, Reprint 2011.
3. Ed William A Goddard III, Donald W Brenner, Sergey Edward Lyshevski, Gerald J Lafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003

## COURSE PLAN

<b>08 EC 6352(C) NANO ELECTRONICS(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<p>MODULE : 1</p> <p><b>Introduction:</b> Overview of nano science and engineering. Development milestones in micro fabrication and electronic industry. Moores law and continued miniaturization., Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nano meter length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nano materials, ordering of nano systems.</p>	<b>6</b>	<b>15</b>
<p>MODULE : 2</p> <p><b>Characterization:</b> Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk, surface, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties</p>	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<p>MODULE : 3</p> <p><b>.Inorganic semiconductor nanostructures:</b> overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states.</p>	<b>6</b>	<b>15</b>
<p>MODULE : 4</p> <p><b>Fabrication techniques:</b> requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved edge over growth, growth of vicinal substrates, strain induced dots and wires, electro statically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nano crystals, collidal quantum dots, self-assembly techniques.</p>	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<p>MODULE : 5</p> <p><b>Physical processes:</b> modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural <b>Methods of measuring properties:structure:atomic,cystallography,microscopy,spectroscopy.</b> Properties of</p>	<b>7</b>	<b>20</b>

nanoparticles: metal nano clusters, semiconducting nano particles, rare gas and molecular clusters, methods of synthesis(RF, chemical, thermolysis, pulsed laser methods)		
<p>MODULE : 6</p> <p>Carbon nanostructures and its applications(field emission and shielding, computers, fuel cells, sensors, catalysis).Self assembling nanostructure molecular materials and devices: building blocks, principles of self assembly, methods to prepare and pattern nanoparticles, template nanostructures, liquid crystal meso phases. Nanomagnetic materials and devices: magnetism, materials, magneto resistance, nanomagnetism in technology, challenges facing nanomagnetism.<b>Applications:</b> Injection lasers, quantum cascade lasers, single photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS.</p>	<b>8</b>	<b>20</b>

### **08 EC6362 MINI PROJECT**

**Pre-requisites: Nil**

**Credits: 0-0-4: 2**

**Year: 2015**

The students have to do a mini project during the second semester itself. The mini project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to do their project outside the parent institute. The mini project should be in the field of Electronics & Communication Engineering and particularly relevant to the specialization of VLSI Design. The students have to submit a report of the undergone project and present the contents of the report before the evaluation committee constituted by the Department. An internal evaluation will be conducted for examining the quality and authenticity of contents of the report and award the marks at the end of the semester.

**08 EC 6372 TESTING & VERIFICATION OF VLSI CIRCUITS –LABORATORY (L-T-P: 3-0-0)****CREDITS:2****COURSE PLAN**

<b>08 EC 6372 TESTING &amp; VERIFICATION OF VLSI CIRCUITS –LABORATORY (L-T-P : 3-0-0) CREDITS:2</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
MODULE : 1 1. Verilog Simulation and RTL Verification a) Memory b) Clock Divider and Address Counter c) n-Bit Binary Counter and RTL Verification 2. Finite State Machines Implement and Verify Using Verilog File I/O 3. Different types of TBs for memory and adder/subtractor	<b>13</b>	<b>15</b>
MODULE : 2 1. Basic Verification environment for FIFO/UART 2. Verification Planning for FIFO/UART a) Development of the test cases as per the verification plan b) Generation and Analysis of Code coverage Reports 3. Writing assertions for FIFO	<b>13</b>	<b>15</b>



## **THIRD SEMESTER**

### **08 EC 7313(A)FPGA ARCHITECTURE AND APPLICATIONS**

**Pre-requisites: Nil**

**Credits: 3-0-0: 3**

**Year: 2015**

#### **Course Objectives:**

- To impart the idea of programmable logic devices,FPGA's,FSM
- It also give the idea about system level design

#### **Syllabus**

Overview of programmable logic devices,FPGA'S,finite state machines,architectures,petrinets,system level design,EDAtool.Casestudies,design consideration using FPGA parallel adder cell

#### **Course Outcome:**

On successful completion of this subject, the student should be capable of

- Understanding about Programmable logic devices
- Understanding about system level design

#### **Text Books:**

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.
3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

#### **REFERENCE BOOKS:**

1. Digital Design Using Field Programmable Gate Array, P.K. Chan & S. Mourad, 1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, 2007, BS

## COURSE PLAN

<b>08 EC 7313(A): FPGA ARCHITECTURE AND APPLICATIONS (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming. Applications and Implementation of MSI circuits using Programmable logic Devices.	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Introduction to advanced FPGAs: Xilinx Virtex and ALTERA Stratix. Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> FSM Architectures: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> System Level Design: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs. Case studies: Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.	<b>8</b>	<b>20</b>

# 08 EC 7313(B) MIXED SIGNAL SYSTEM DESIGN

Pre-requisites: Nil

Credits: 3-0-0: 3

Year: 2015

## Course Objectives:

- To fundamentals concept about PN junction, bipolar devices etc
- It also give the idea about Digital and analog sub circuits

## Syllabus

Introduction about basic active components, digital sub circuits, analog sub circuits, Data converters: DAC, ADC, oversampling data converters

## Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze the Programmable logic devices
- Analyze the system level design

## Text Books:

1. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3<sup>rd</sup> edition, John Wiley & Sons.
2. Jacob Baker, "CMOS Mixed-Signal circuit design", A John Willy & Sons, inc., publications, 2003.
3. Professor Bernhard Boser -"Analysis and Design of VLSI Analog-Digital Interface Integrated Circuits" "Addison Wisely publications" (1991).

## REFERENCE BOOKS:

1. D A John, Ken Martin, Analog Integrated Circuit Design, 1<sup>st</sup> Edition, John Wiley
2. CMOS Analog Circuit Design, 2<sup>nd</sup> edition; by: Allen, Phillip E, Holberg, Douglas R, Oxford University Press, (Indian Edition
3. Ken Martin, Digital Integrated Circuit Design, John Wiley

## COURSE PLAN

<b>08 EC 7313(B): MIXED SIGNAL SYSTEM DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> <b>Introduction:</b> PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing, Example of Analog Mixed Signal Circuit Design	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Example of Analog Mixed Signal Circuit Design <b>Digital Sub Circuits:</b> CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Encoders, decoders. Digital Circuits like ALU, Comparator, Parity generator, Timer, PWM,SRAM and DRAM, CAM, <b>Analog Sub circuits:</b> Ideal Operational Amplifier	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Inverting and Non-inverting configuration Differential amplifier basics .VCO, PLL, Comparator characteristics, two stage open loop comparator	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Switched capacitor fundamentals, Switched capacitor amplifier <b>Data Converters:</b> <b>DAC :</b> Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> <b>ADC :</b> Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit, Quantization error, Concept of over sampling, Counting ADC, Tracking ADC, Successive approximation ADC, Flash ADC, Dual Slope ADC <b>Over sampling Data Converters :</b> Over sampling fundamentals, Delta –Sigma Converter basics, $\Sigma$ Modulator	<b>8</b>	<b>20</b>

## 08 EC 7313(C) ASIC DESIGN

Pre-requisites: Nil

Credits: 3-0-0: 3  
Year: 2015

### Course Objectives:

- To impart the idea of ASIC, Data logic cells
- It also give the idea about programmable logic cell

### Syllabus

Introduction about Asic FPGA design flow, SIC cell libraries, data logic cells, ASIC library design ,Low-level design entry, Programmable ASIC, Introduction about low level design language ,ASIC construction floor planning and placement and routing

### Course Outcome:

On successful completion of this subject, the student should be capable of

- Getting the idea about ASIC
- Applying ASIC construction floor planning and placement and routing

### Text Books:

1. M.J.S .Smith, - "**Application - Specific Integrated Circuits**" – Pearson Education, 2003.
2. Jose E.France, Yannis Tsvividis, "**Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing**", Prentice Hall, 1994,
3. Malcolm R.Haskard; Lan. C. May, "**Analog VLSI Design – NMO Sand CMOS**", Prentice Hall, 1998.
4. Mohammed Ismail and Terri Fiez, "**Analog VLSI Signal and Information Processing**", McGraw Hill, 1994

## COURSE PLAN

<b>08 EC 7313(C) ASIC DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> <b>introduction:</b> Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channelled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, SIC cell libraries	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> <b>Data Logic Cells:</b> Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers, <b>ASIC Library Design:</b> Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> <b>Low-Level Design Entry:</b> Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S,connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation.	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> <b>Programmable ASIC:</b> programmable ASIC logic cell, ASIC I/O cell. <b>A Brief Introduction to Low Level Design Language:</b> an introduction to EDIF, PLA Tools, an introduction to CFI designs representation.	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Half gate ASIC. Introduction to Synthesis and Simulation. <b>ASIC Construction Floor Planning and Placement And Routing:</b> Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.	<b>8</b>	<b>20</b>

## 08 EC 7323(A) SYSTEM VERILOG

Pre-requisites: Nil

Credits: 3-0-0: 3

Year: 2015

### Course Objectives:

- To impart the basics of introduction to functional verification languages
- Make a idea about object oriented programming

### Syllabus

Introduction to functional verification languages, classes and objects ,inheritance, system verilog assertion, Basics of properties and sequences, coverage driven verification and functional coverage in SV

### Course Outcome:

On successful completion of this subject, the student should be capable of

- Applying functional verification languages
- Applying the idea about system verilog

### Text Books:

1. "System Verilog for Design" : A Guide to Using System Verilog for Hardware Design and Modeling Sutherland, Stuart, David mann, Simon, Flake, Peter 2nd ed., 2006
2. "SystemVerilog for Verification": A Guide to Learning the Testbench Language Features, Chris Spear, 2006
3. "Hardware Verification with System Verilog": An Object-Oriented Framework Mintz, Mike, Ekendahl, Robert 2007

### REFERENCE BOOKS:

1. "Writing Test benches using System Verilog" Bergeron, Janick 2006,
2. "A Practical Guide for System Verilog Assertions" Meyyappan Ramanathan

## COURSE PLAN

<b>08 EC 7323(A) SYSTEM VERILOG (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> Introduction to functional verification languages, Introduction to System Verilog, System Verilog data types	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> System Verilog procedures, Interfaces and modports, System Verilog routines.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Introduction to object oriented programming, Classes and Objects, Inheritance, Composition, Inheritance v/s composition,	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Virtual methods. Parameterized classes, Virtual interface, Using OOP for verification, System Verilog Verification Constructs	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> System Verilog Assertions: Introduction to assertion, Overview of properties and assertion, Basics of properties and sequences, Advanced properties and sequences, Assertions in design and formal verification, some guidelines in assertion writing.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> Coverage Driven Verification and functional coverage in SV: Coverage Driven Verification, Coverage Metrics, Code Coverage, Introduction to functional coverage, Functional coverage constructs, Assertion Coverage, Coverage measurement, Coverage Analysis SV and C interfacing: Direct Programming Interface (DPI)	<b>8</b>	<b>20</b>



# 08 EC 7323(B) HARDWARE SOFTWARE CO-DESIGN

Pre-requisites: Nil

Credits: 3-0-0: 3

Year: 2015

## Course Objectives:

- To impart the basis of hardware software co design
- It also give the object oriented techniques in hard ware design

## Syllabus

Introduction, Hardware software background, Co-design concepts, Methodology for co-design,an abstract hardware and software model, object oriented techniques in hardware design

## Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze how to implements hardware software co design
- Applying the idea about object oriented techniques

## Text Books:

1. Sanjaya Kumar, James H. Ayler“The Co-design of Embedded Systems: A Unified Hardware Software Representation”, Kluwer Academic Publisher, 2002 .
2. H. Kopetz, “Real-Time Systems”, Kluwer, 1997.
3. R. Gupta, “Co-synthesis of Hardware and Software for Embedded Systems”, Kluwer 1995.

## REFERENCE BOOKS:

1. S. Allworth, “Introduction to Real-time Software Design”, Springer-Verlag, 1984.
2. C. M. Krishna, K. Shin, “Real-time Systems”, Mc-Graw Hill, 1997
3. Peter Marwedel, G. Goosens, “Code Generation for Embedded Processors”, Kluwer Academic Publishers, 1995.

## COURSE PLAN

<b>08 EC 7323(B) HARDWARE SOFTWARE CO-DESIGN (L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> <b>Introduction:</b> Motivation hardware & software co-design, system design consideration, research scope & overviews	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> <b>Hardware Software back ground:</b> Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> <b>Co-design Concepts:</b> Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software tradeoffs, co-design.	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> <b>Methodology for Co-Design:</b> Amount of unification, general consideration & basic philosophies, a framework for co-design Unified Representation for Hardware & Software: Benefits of unified representation, modeling concepts.	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> <b>An Abstract Hardware &amp; Software Model:</b> Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model Performance Evaluation: Application of the abstract Hardware & Software model, examples of performance evaluation	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> <b>Object Oriented Techniques in Hardware Design:</b> Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example.	<b>8</b>	<b>20</b>

## 08 EC 7323(C) VLSI SIGNAL PROCESSING

Pre-requisites: Nil

Credits: 3-0-0: 3

Year: 2015

### Course Objectives:

- To impart the fundamentals and overview of DSP concepts
- It give the description about of digital filters

### Syllabus

An overview of DSP concepts, Algorithm for fast convolution, Pipeline interleaving in digital filters, State variable description of digital filters

### Course Outcome:

On successful completion of this subject, the student should be capable of

- Analyze the DSP
- Applying the idea of digital filters

### Text Books:

1. K.K. Parhi, VLSI Digital Signal Processing Systems, John-Wiley, 1999.
2. Pirsch, P., Architectures for Digital Signal Processing, Wiley, 1999.

### REFERENCE BOOKS:

1. S. Allworth, "Introduction to Real-time Software Design", Springer-Verlag, 1984.
2. C. M. Krishna, K. Shin, "Real-time Systems", Mc-Graw Hill, 1997
3. Peter Marwedel, G. Goosens, "Code Generation for Embedded Processors", Kluwer Academic Publishers, 1995.

## COURSE PLAN

<b>08 EC 7323(B) VLSI SIGNAL PROCESSING(L-T-P : 3-0-0) CREDITS:3</b>		
<b>MODULES</b>	<b>Contact hours</b>	<b>Sem.Exam Marks;%</b>
<b>MODULE : 1</b> An overview of DSP concepts-Linear system theory- DFT, FFT- realization of digital filters- Typical DSP algorithms- DSP applications	<b>6</b>	<b>15</b>
<b>MODULE : 2</b> Data flow graph representation of DSP algorithm.- Loop bound and iteration bound Retiming and its applications.	<b>6</b>	<b>15</b>
<b>FIRST INTERNAL TEST</b>		
<b>MODULE : 3</b> Algorithms for fast convolution- Algorithmic strength reduction in filters and transforms- DCT and inverse DCT- Parallel FIR filters	<b>6</b>	<b>15</b>
<b>MODULE : 4</b> Pipelining of FIR filters- Parallel processing- Pipelining and parallel processing for low power. Pipeline interleaving in digital filters	<b>6</b>	<b>15</b>
<b>SECOND INTERNAL TEST</b>		
<b>MODULE : 5</b> Pipelining and parallel processing for IIR filters-Low power IIR filter design using pipelining and parallel processing- Pipelined adaptive digital filters.	<b>7</b>	<b>20</b>
<b>MODULE : 6</b> State variable description of digital filters- Round off noise computation using state variable description- Scaling using slow-down, retiming and pipelining.	<b>8</b>	<b>20</b>

## 08 EC 7333 SEMINAR

Pre-requisites: Nil

Credit : 0-0-2 : 2

Year: 2015

### ***Objective:***

*To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.*

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 30 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students. Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

## 08 EC 7343 PROJECT PHASE I

Pre-requisites: Nil

Credit : 0-0-12 : 6

Year: 2015

### **Objective:**

*To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.*

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

The student is required to undertake the project phase 1 during the third semester and the same is continued in the 4<sup>th</sup> semester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4<sup>th</sup> semester. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

## **SEMESTER 4**

### **08 EC 7314 PROJECT PHASE II**

**Pre-requisites: Nil**

**Credit : 0-0-21 : 12**  
**Year: 2015**

*Objective:*

To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.

Project phase II is a continuation of project phase I started in the third semester. There would be two reviews in the fourth semester, first in the middle of the semester and the second at the end of the semester. First review is to evaluate the progress of the work, presentation and discussion. Second review would be a pre -submission presentation before the evaluation committee to assess the quality and quantum of the work done. This would be a pre qualifying exercise for the students for getting approval by the departmental committee for the submission of the thesis. At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis.